Claims

1. A method for self-tuning an L-C filter network comprising

   A phase-frequency detector with a fixed reference frequency input and a frequency-divided oscillator input. The output of the phase detector is connected to

   A digital loop filter whose output is connected to

   A digital-to-analog converter that generates a voltage to tune the capacitors of

   A voltage-controlled oscillator based on an L-C resonant circuit. The output of the voltage-controlled oscillator connect to

   A frequency divider whose output connects to an input of the phase detector.

   A L-C filter network comprising a tunable main L-C filter wherein the capacitors in the filter are controlled by a tuning voltage that is used to tune the voltage-controlled oscillator.

2. The method of claim 1 wherein the tunable capacitors are based on varactors.
3. The method of claim 1 wherein the tunable capacitors are based on MOS capacitors.
4. The method of claim 1 wherein the inductors are based on on-chip spiral inductors.

5. The method of claim 1 wherein the inductors are based on bonding wires.
6. The method of claim 1 wherein the phase-locked looped can be powered down, and the value of the loop filter output can continue to tune the main L-C filter.
7. The method of claim 1 wherein the main L-C filter is a ladder type.
8. The method of claim 1 wherein the main L-C filter is a two-pole resonant circuit.
9. The method of claim 1 wherein the main L-C filter forms a low-pass filter.
10. The method of claim 1 wherein the main L-C filter forms a high-pass filter.
11. The method of claim 1 wherein the main L-C filter forms a band-pass filter.
12. The method of claim 1 wherein the main L-C filter forms a band-stop filter.
13. The method of claim 1 wherein the main L-C filter is used in a radio frequency system.
14. The method of claim 1 wherein the circuits are implemented in a CMOS technology.
15. The method of claim 1 wherein the circuits are implemented in a bipolar technology.
16. The method of claim 1 wherein the circuits are implemented in other semiconductor process technologies.
17. The method of claim 1 wherein the digital loop filter is implemented by a digital counter.
18. The method of claim 1 wherein the L-C filter includes resistors.

19. The method of claim 1 wherein the number of capacitor elements in the main L-C filter are N, where N is an integer.
20. The method of claim 1 wherein the number of inductor elements in the main L-C filter are M, where M is an integer.
21. The method of claim 1 wherein the number of resistor elements in the main L-C filter are J, where J is an integer.
22. The method of claim 1 wherein the tuning voltage is used to control multiple L-C filter networks.
23. The method of claim 1 wherein the circuits are fully differential.
24. The method of claim 1 wherein the circuits are single-ended.